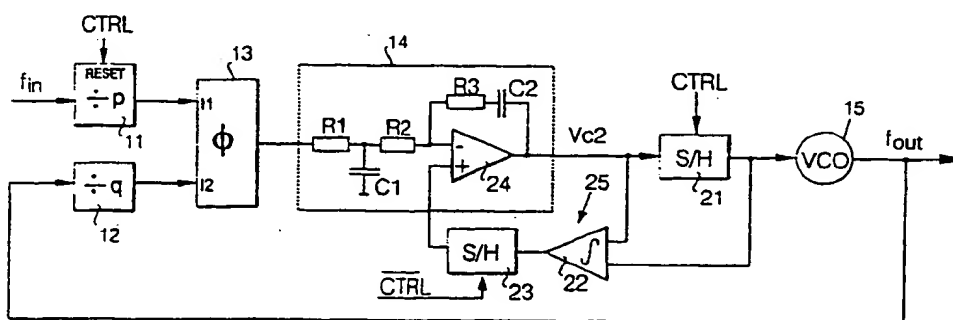




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(54) Title: METHOD FOR CONTROLLING A PHASE-LOCKED LOOP, AND A PHASE-LOCKED LOOP



(57) Abstract

The invention relates to a method for controlling a phase-locked loop in a locking situation, and to a phase-locked loop. The loop comprises a phase detector (13), a loop filter (14) and a voltage-controlled oscillator (15) connected in succession, a feedback path being established from the output of the oscillator to a second input (12) in the phase detector. In response to a change causing a currently used input signal to become inadequate for locking, the signal connected from the loop filter (14) to the oscillator (15) is frozen to a constant value, and in response to a change causing a currently used signal to become again adequate for locking, the freezing is removed. In the method, in order that the locking would take place directly, without any sudden phase changes, (a) the output signal of the loop filter (14) is additionally maintained substantially at said constant value by means of the feedback loop (25; 45) in response to a change causing the currently used input signal to become inadequate for locking; and (b) the control provided by said feedback loop for the loop filter (14) is frozen substantially at its current value in response to a change causing the signal to become again adequate for locking.

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Method for controlling a phase-locked loop, and a phase-locked loop

5 The invention relates to a method according to the preamble of attached claim 1 for controlling a phase-locked loop in a locking situation, and to a phase-locked loop according to the preamble of attached claim 6. As used herein, the *locking situation* refers to a situation where the input signal of the loop is disconnected or replaced with another
10 signal, and the loop is thereafter re-locked, either to a new or the old input signal. The solution according to the invention is usable particularly in the generation of synchronizing signals for digital tele-
15 communication systems.

It may become necessary to use synchronizing clocks as independent adjustable oscillators, e.g. when the synchronizing clock has lost its input signal. In telecommunication equipment complying with
20 the SDH standard, for instance, the system clock is forced to remain at the frequency at which it was when it lost its input signal. The clock has to operate independently until it can be re-locked to a synchronizing signal. No significant changes in phase are
25 allowed in the output signal during re-locking; this requirement has also to be met when the input signal is replaced with another signal.

When an analog phase-locked loop is re-locked to the input signal, or the input signal is replaced
30 with another signal, considerable phase changes may occur, particularly if a long chain of frequency dividers precedes the phase detector of the loop. The magnitude of the phase change depends both (a) on the phase difference between the output signal and the
35 input signal of the phase-locked loop at the switching

moment and (b) on the properties of the loop filter and the phase detector.

Figure 1 shows a phase-locked loop (PLL) 10 known *per se* in its general configuration, comprising a phase detector 13, a lowpass-type loop filter 14 having an input to which the output signal of the phase detector is connected, and a voltage-controlled oscillator 15 arranged to be controlled by the loop filter. A signal is applied to both inputs, I1 and I2, of the phase detector through a frequency divider 11 and 12, respectively. A signal f_{in} is applied as an input signal to the frequency divider 11, which divides the frequency of the signal f_{in} by the integer p so that a signal having a frequency f_{in}/p (in this text, reference f refers both to the signal and to its frequency) is applied to the first input I1 of the phase detector 13. The output signal f_{out} of the oscillator 15 is applied through the frequency divider 12 back to the second input I2 of the phase detector 13. The phase detector thus compares the phase of the signal having the frequency f_{in}/p with the phase of the signal having the frequency f_{out}/q and generates a control signal V_{c1} proportional to their phase difference. This control signal is lowpass-filtered in the loop filter 14, and the filtered signal V_{c2} is applied to the oscillator 15 to control it. When the loop is locked, Formula (1) is valid for the output signal of the loop:

$$(1) f_{out} = \frac{q}{p} f_{in}$$

that is, the frequency of the output signal is the frequency of the input signal multiplied with the number q/p .

In the phase-locked loop, the phase of the input signal fin can be adjusted suitably before switching so that the phase shift of the input signals of the phase detector will correspond to the phase shift of the locked state, provided that the loop filter has a sufficiently high DC voltage gain, so that the phase difference remains unchanged despite small frequency changes. In the case shown in Figure 1, for instance, where the input signal is followed by a divider chain 11, the phase adjustment can be performed with the accuracy of one clock period of the input signal by initializing the divider 11 (by resetting its counter) and enabling it appropriately so that a desired phase shift will be obtained between the input signals. For instance, if the frequency of the input signal is 2 MHz, the phase can be set with the accuracy of 500 ns. If this accuracy is not adequate, it is possible, for instance, to increase the frequency of the input signal by a separate multiplier and correct the value of the divisor p correspondingly.

In spite of the phase adjustment of the input signal, there may still occur large instantaneous phase changes in the output of the phase-locked loop. This is because the loop filter may have drifted to the limit of its operating range due to the lack of feedback. (Feedback disappears when the input signal is missing). In a locking situation, it thus takes some time before the filter is again in the normal state.

Even though the phase detector provides zero output when the input signal is missing, even an extremely low offset voltage drives the loop filter to the limit of its operating range if the loop filter has a high DC voltage gain. (The offset voltage is the deviation of the control voltage applied to the loop

filter from a value which would maintain the output voltage of the loop filter at a value corresponding to the nominal frequency.) In practice, even thermal drift alone may prevent direct calibration of the offset voltage with a sufficient accuracy.

It is further to be mentioned that the requirements set e.g. in the CCITT recommendation G.81s for the system clock of a SDH network node cannot be met by means of an analog phase-locked loop without a more accurate phasing mechanism.

Phase errors can be prevented by means of a solution in which the actual phase-locked loop is followed by another (wide-bandwidth) phase-locked loop, the output frequency of which is frozen when the input signal is disconnected. During re-locking, the actual phase-locked loop is first allowed to lock and only after this the other phase-locked loop is connected to track the actual phase-locked loop. A drawback of this solution is that the entire system is not locked until the actual phase-locked loop has locked, which may take a very long time.

Another solution is to increase the bandwidth of the loop filter in a locking situation, which as such will not prevent phase errors but merely speeds up the locking.

The object of the present invention is to avoid the above-described problems and to provide a solution, which allows the phase-locked loop to continue from the same phase as accurately as possible on re-locking. This is achieved by means of a method and a phase-locked loop according to the invention, of which the method is characterized by what is described in the characterizing portion of attached claim 1, and the phase-locked loop is characterized by what is described in the characterizing portion of attached

claim 6.

The idea of the invention is to maintain the loop filter as accurately as possible in the state where it was when the loop was locked to the input signal, when the input signal is disconnected or becomes inadequate in quality, that is, to prevent the loop filter from "drifting to the limit", from which the restoration to the normal state takes a certain time. In other words, in the invention, the above-mentioned offset voltage is reset in a state in which the phase lock is not locked.

The solution according to the invention prevents any sudden phase changes during the re-locking of the loop, and it allows the output signal to be immediately at its final phase, the accuracy of which depends only on the accuracy of the phase adjustment of the input signal. If the new locking frequency deviates from the old one, a properly designed loop drifts directly towards the new frequency without any sudden phase changes.

In the following the invention and its preferred embodiments will be described by way of example with reference to Figures 2 to 5 in the attached drawings, in which

Figure 1 shows a phase-locked loop known per se in its general configuration;

Figure 2 shows a first embodiment of the phase-locked loop according to the invention;

Figure 3 shows an alternative embodiment for the embodiment shown in Figure 2;

Figure 4 shows another alternative embodiment for the embodiment shown in Figure 2; and

Figure 5 shows an additional embodiment for the solutions shown in Figures 2, 3 and 4.

In the solution according to the present inven-

tion, the input signal is phased as described above (if the inputs of the phase detector comprise frequency dividers), in addition to which the loop filter is prevented from drifting to the limit of its operating range. As the output of the loop filter is maintained unchanged when the input signal is disconnected, the following locking takes place directly without any sudden phase changes.

Figure 2 shows the first embodiment of the phase-locked loop according to the invention. The same reference numerals as in Figure 1 are used for corresponding parts. In this specific case, the loop filter, shown in greater detail in Figure 2 than in Figure 1, comprises an inverting filter 14 having an operational amplifier 24, resistors R1 to R3, and capacitances C1 and C2, of which the last-mentioned establishes (in series) with the resistor R3 a feedback loop for the operational amplifier. The more detailed implementation of the loop filter may vary in many ways within the scope of solutions known per se. The only requirement set for the filter is that it should be active, having an adequate DC voltage gain, in order that small frequency changes would not cause any significant phase changes.

A sampling circuit 21 is positioned between the loop filter 14 and the oscillator 15. It samples the output signal of the loop filter at a predetermined sampling frequency dependent on the application used; stores sample values in a memory over a predetermined time period; and connects an analog control voltage to the oscillator. It is advisable that the sampling circuit is infinite in type, i.e. it should in principle be able to maintain the value of its output signal endlessly. The sampling circuit is implemented in a manner known per se by means of A/D and D/A

converters and registers.

According to the invention, a second feedback is established from the output of the loop filter to the input of the loop filter or the phase detector. The purpose of this second feedback is to replace the actual feedback loop of the phase-locked loop formed by the oscillator and the phase detector when the input signal is disconnected. By means of the replacing feedback loop the output of the filter is maintained unchanged in spite of the disconnection of the input signal. The following requirements are set for the replacing feedback loop:

- The DC voltage gain has to be high in order that the output of the loop filter would remain unchanged (equal to the frozen control voltage of the oscillator) as accurately as possible.

- The circuit has to be stable even when the feedback loop is replacing the actual loop formed by the oscillator and the phase detector. The replacing feedback loop thus has to be integrating, like the actual loop (the voltage-controlled oscillator).

- It has to be possible to "freeze" the control supplied by the feedback loop (to the input of the filter or the phase detector, as will be described below) when the phase-locked loop is again locked to an input signal of adequate quality. Otherwise a change in this control would appear as an undesired phase change in the output of the phase-locked loop.

The replacing feedback loop according to the invention has a wide range of different implementations, which will be described below with reference to Figures 2 to 4 (in other respects, the embodiments of Figures 3 and 4 correspond to the solution shown in Figure 2).

In the first embodiment shown in Figure 2, the

replacing feedback loop 25 is established through an integrating amplifier 22 and a second sampling circuit 23 to the input of the loop filter. The output of the loop filter 14 is connected to the first input of the amplifier 22, and the output of the first sampling circuit 21 (which output is also connected to control the oscillator) to the second amplifier input. The output of the amplifier is connected to the second sampling circuit 23, the output of which is connected to a non-inverting input of the operational amplifier 24 of the loop filter. When the input signal (f_{in}) is disconnected, the amplifier 22 controls the loop filter through the sampling circuit 23 so that the filter output remains unchanged, that is, equal to the frozen control voltage of the oscillator. Upon re-locking to an input signal of adequate quality, the control supplied by the replacing feedback loop to the loop filter is in turn frozen to its current value by means of the sampling circuit 23. The sampling circuit 23 has to be "permanent" in type, i.e. of the same kind as the first sampling circuit 21 (controlling the oscillator) described above.

Figure 3 shows another alternative for the replacing feedback loop 25. In this embodiment, the integrating amplifier and the second sampling circuit are replaced with a comparator 32 and an adjustable voltage supply 33, the value of the output voltage of which the comparator 32 is able to control so as to increase or decrease it. The comparator compares the output signal of the loop filter with the frozen control voltage of the oscillator and controls the voltage supply 33 so that the output signal of the loop filter remains unchanged. The adjusting rate of the voltage supply is selected so that the loop formed by the filter and the replacing feedback remains

stable. The adjustable voltage supply 33 can be realized e.g. by an up/down counter and a D/A converter, or alternatively by a circuit which increases or decreases its pulse ratio under the control of the
5 comparator and a lowpass filter following the circuit.

When the phase-locked loop shown in Figure 3 is re-locked to an input signal of adequate quality, the output voltage of the D/A converter or the pulse ratio adjustment, respectively, is "frozen" to the value
10 which it had at the moment of change.

The above-described feedback circuits control the input of the loop filter. The feedback circuit may also control the phase of signals before the phase detector. Figure 4 illustrates this embodiment, where
15 a phase adjustment unit 40 is provided between the frequency dividers and the phase detector. In this case, the replacing feedback loop is indicated with reference numeral 45. Phase adjustment requires that there should be a signal at both inputs of the phase
20 detector, but as the output of the divider 11 is reset when the input signal is missing, this has to be replaced with a signal having the same frequency and phase as when the phase-locked loop is locked in the stable state (the phase difference between the signals
25 is equal to the nominal phase shift of the phase detector in the stable state). The replacing signal can be produced easily by means of the divider 12, e.g. simply by adding a phase shift to its output signal in a phase shift means 41 and connecting a
30 replacing signal by means of a switch 42 in place of the output signal of the divider 11. (In the example shown in Figure 4, the nominal phase shift of the phase detector is 90 degrees.) The mutual phase of the signals is adjusted (by adjusting the delay of one of
35 the signals in the adjustment unit 40) before the

phase detector under the control of a phase control signal PC supplied by the comparator 32 so that the output signal of the loop filter remains unchanged.

5 When the circuit of this embodiment again receives an input signal of adequate quality, to which it is locked, the output of the divider 11 is released to operate normally and the adjusted phase difference is "frozen" to its current value.

10 The operation of the phase-locked loop according to the invention will be described below in greater detail by using the embodiment shown in Figure 2 as an example. In the other embodiments shown, corresponding feedback means operate similarly.

15 In the normal state the output signal fout of the loop is locked to the input signal fin, whereby there is a certain constant phase difference between the input signals of the phase detector. The first sampling circuit 21 takes samples into the memory and its output signal forms the control voltage of the
20 oscillator. In this situation the first sampling circuit 21 is thus transparent, i.e. it connects the output signal of the loop filter 14 substantially as such to the oscillator 15.

25 In the normal state, the value of the output signal of the second sampling circuit 23 has been frozen to a constant value, i.e. the feedback loop 25 does not actually exist, but the phase-locked loop operates in a manner known per se by means of its actual feedback path.

30 When the input signal is disconnected, or when it is replaced with another signal, the counter of the divider 11 is reset (so that the divider will not allow a signal to pass through it). When the input signal is disconnected (or replaced), the output
35 signal of the first sampling circuit (the control of

the oscillator) is also frozen immediately to a certain constant value. This constant value, which is determined in the first sampling circuit 21, is preferably a time average calculated for the control signal Vc2 (the output signal of the filter) over a longer period of time. The value that occurred immediately before the input signal was disconnected or replaced is likely to be incorrect, so that it is advisable to calculate the time average as described above instead of using this value.

An indication that the input signal has been disconnected or become inadequate in quality (or that the input signal has been restored or become adequate in quality) is provided in a manner known *per se*, e.g. on the basis of the state and alarm data of the telecommunication system.

At the same time as the input signal is disconnected, or replaced with another signal, the above-mentioned separate feedback loop 25 replacing the actual, disconnected loop is established for the loop filter 14. The feedback loop 25 maintains the outputs of the loop filter and the first sampling circuit equal by adjusting the DC control voltage of the filter. In the stable state, the DC control voltage of the filter is the same as what it was in the normal locked state. In this unlocked state, the sampling circuit 23 of the feedback loop is transparent, i.e. it connects the output signal of the feedback amplifier 22 substantially as such to the loop filter.

When an indication is again received that the input signal is adequate, the counter of the frequency divider 11 is enabled in an appropriate phase so that the phase shift of the input signals of the phase detector corresponds to the phase shift of the locked state. At the same time the output signal of the

second sampling circuit 23 is frozen to its current value (which disconnects the feedback loop 25) and the first sampling circuit is released to operate normally so that the output signal of the filter appears again at its output. In Figure 2, the control signal freezing the first sampling circuit is indicated with reference CTRL. Signal CTRL controlling the second sampling circuit 23 is the complementary signal of the control signal CTRL, as the second sampling circuit is released when the first sampling circuit is frozen, and vice versa.

When the phase-locked loop is started for the first time, the procedure is initially the same as with a missing input signal. A constant value, which is a guess as good as possible at the control voltage required by the locking state, is written in advance into the sampling circuit 21 controlling the oscillator. The feedback amplifier 22 presets the filter into a state as close to the right one as possible and at the same time the output signal of the sampling circuit 23 following the DC control voltage is automatically set to the right value. Only after this the loop is allowed to lock.

If the output signal of the divider 11 or 12 is asymmetrical with respect to its pulse ratio, the phasing will not operate accurately as such, as the asymmetry causes an offset voltage jump to occur at the output of the phase detector when the input signal is connected to the phase detector (the divider 11 is released). The asymmetrical output signal of the dividers 11 and 12 can, however, be compensated for by simultaneously adding an offset voltage of the same magnitude to the input of the loop filter. This alternative is shown in Figure 5 by using the embodiment shown in Figure 2 as a starting point. A lowpass

filter AP similar to the prefilter formed by the resistor R1 and the capacitor C1 is formed between the output of the sampling circuit 23 and the loop filter 14 by means of a resistor R4 and a capacitor C3 in order that the compensating offset voltage would be connected to the loop filter through a similar time constant as the voltage jump from the phase detector. The output signal of the sampling circuit 23 is connected by means of a separate switch 26 through a lowpass filter to the loop filter. When the phase-locked loop is locked, the switch is displaced into the position shown in Figure 5 so that a low offset voltage (typically a few mV in magnitude) formed by the offset voltage supply 27 is added to the filter input. When the phase-locked loop is unlocked, the switch 26 is in the opposite position, so that the output voltage of the sampling circuit will be switched directly to the lowpass filter (without the addition of the offset voltage). The switch 26 is controlled by the same control signal as the sampling circuit 23. In other respects, the preferred embodiment shown in Figure 5 corresponds to the first embodiment shown in Figure 2, but the solution may equally well be applied to the embodiments shown in Figures 3 and 4.

Still another advantage of the solution according to the invention is that an indication that the filter has settled (which, in practice, is highly significant, particularly if the time constant of the loop filter is high) is obtained easily e.g. by monitoring the output signal of the feedback amplifier or the comparator.

Even though the invention has been described above with reference to the examples of the attached drawings, it is self-evident that the invention is not

related to it, but it can be modified within the inventive idea defined above and in the attached claims. For instance, the loop need not necessarily have the frequency dividers (11 or 12) preceding the phase
5 detector (in such a case, however, the circuit has to include a latch circuit disabling the signal of inadequate quality before the phase detector). If there is no frequency divider 11 dividing the frequency of the input signal, the above-mentioned resetting and
10 enabling of the counter are also omitted; in other respects the circuit operates as described above. If the divider 11 or 12 is omitted, it, however, has to be attended to that the input signals are symmetrical in pulse ratio or alternatively, the compensation
15 described above has to be performed.

Claims:

1. Method for controlling a phase-locked loop in a locking situation, the loop comprising a phase detector (13), a loop filter (14) and a voltage-controlled oscillator (15) connected in succession, a feedback path being established from the output of the oscillator to a second input (I2) in the phase detector, and an input signal to which the loop is locked being applied to a first input (I1) in the phase detector (13), and, in response to a change causing a currently used input signal to become inadequate for locking, the signal connected from the loop filter (14) to the oscillator (15) is frozen to a constant value, and in response to a change causing the signal to become again adequate for locking, said freezing is removed, characterized in that the output signal of the loop filter (14) is additionally maintained substantially at said constant value by means of a feedback loop (25; 45) in response to a change causing the currently used input signal to become inadequate for locking; and

the control provided by said feedback loop of the loop filter (14) is frozen substantially at its current value in response to a change causing the signal to become again adequate for locking.

2. Method according to claim 1, characterized in that the output signal of the loop filter is maintained substantially at said constant value by establishing a new feedback loop (25) from the output of the loop filter to its input.

3. Method according to claim 2, characterized in that the output signal of the loop filter is maintained substantially at said constant value by establishing a new feedback loop (45), by

means of which the mutual phase of signals applied to the phase detector (13) is adjusted.

4. Method according to claim 1, characterized in that a time average of the output signal (Vc2) of the filter (14) calculated over a time period of a predetermined length is used as said constant value.

5. Method according to claim 1, characterized in that when the phase-locked loop comprises a frequency divider (11) through which the input signal is applied to the phase detector (13),

the counter of the frequency divider is reset in response to a change causing a currently used input signal to become inadequate for locking, and

in response to a change causing a currently used input signal to become adequate for locking, the counter of the frequency divider is enabled so that the phase difference between the input signals of the phase detector immediately corresponds to the nominal phase shift of the phase detector.

6. Phase-locked loop comprising a phase detector (13), a loop filter (14) and a voltage-controlled oscillator (15) connected in succession, a feedback path being established from the output of the oscillator to a second input (I2) in the phase detector; and means (21) for freezing a signal connected from the loop filter (14) to the oscillator (15) to a constant value, characterized in that it further comprises feedback means (25; 45) fed back from the output of the loop filter so that a second feedback path can be established for the phase-locked loop, the second feedback path being operationally connected to maintain the output signal of the loop filter (14) substantially at said constant value.

7. Phase-locked loop according to claim 6,

characterized in that said means for freezing the signal connected to the oscillator (15) to a constant value comprise a sampling circuit (21) including means for calculating the constant value on the basis of sample values.

8. Phase-locked loop according to claim 7, characterized in that said feedback means for maintaining the loop filter at said constant value comprise a feedback amplifier (22) having a first input connected to the output of the loop filter, a second input connected to the output of said sampling circuit (21), and an output which is operationally connected to provide DC control voltage for the loop filter.

9. Phase-locked loop according to claim 8, characterized in that said feedback means for maintaining the loop filter at said constant value further comprise a sampling circuit (23) arranged between the feedback amplifier (22) and the filter (14), the value of the output signal of the sampling circuit being freezable to a constant value.

10. Phase-locked loop according to claim 7, characterized in that said feedback means for maintaining the loop filter at said constant value comprise a comparator (32) having a first input connected to the output of the loop filter (14) and a second input connected to the output of said sampling circuit (21), and an adjustable voltage supply (33), the output signal of the comparator being connected to control the voltage supply, whereby the output of the voltage supply provides DC control voltage for the loop filter (14).

11. Phase-locked loop according to claim 10, characterized in that the adjustable voltage supply (33) comprises means for generating a

signal having an adjustable pulse ratio, and means for lowpass-filtering said signal.

12. Phase-locked loop according to claim 10, characterized in that the adjustable voltage supply (33) comprises an up/down counter and a D/A converter, which is controlled by the counter.

13. Phase-locked loop according to claim 7, characterized in that said feedback means for maintaining the loop filter at said constant value comprise a comparator (32) having a first input connected to the output of the loop filter (14) and a second input connected to the output of said sampling circuit (21), and the output of which is connected to phase-adjusting means (40) provided at the input of the phase detector (13) for adjusting the mutual phase of signals fed to the phase detector.

14. Phase-locked loop according to claim 6, characterized in that it further comprises means (26, 27) for adding a low offset voltage to the input of the loop filter.

AMENDED CLAIMS

[received by the International Bureau on 17 February 1995 (17.02.95); original claims 1,2,3,6 amended; remaining claims unchanged (4 pages)]

1. Method for controlling a phase-locked loop in a locking situation, the loop comprising a phase
5 detector (13), a loop filter (14) and a voltage-controlled oscillator (15) connected in succession, a feedback path being established from the output of the oscillator to a second input (I2) in the phase
10 detector, and an input signal to which the loop is locked being applied to a first input (I1) in the phase detector (13), and

in response to a change causing a currently used input signal to become inadequate for locking, the signal connected from the loop filter (14) to the
15 oscillator (15) is frozen to a constant value and an additional feedback loop is connected to maintain the output signal of the loop filter substantially at said constant value, and

in response to a change causing the signal to
20 become again adequate for locking, said freezing is removed,

c h a r a c t e r i z e d in that

when said additional feedback loop is connected in response to a change causing a currently used input
25 signal to become inadequate for locking, the input of the loop filter is maintained connected to the phase detector and said inadequate signal is disabled before the phase detector; and

the control provided by said additional feedback
30 loop is frozen substantially at its current value in response to a change causing the signal to become again adequate for locking.

2. Method according to claim 1, c h a r a c t e r i z e d in that said additional feedback loop
35 is established from the output of the loop filter to

its input.

3. Method according to claim 1, characterized in that the mutual phase of signals applied to the phase detector (13) is adjusted by means of said additional feedback loop.

4. Method according to claim 1, characterized in that a time average of the output signal (Vc2) of the filter (14) calculated over a time period of a predetermined length is used as said constant value.

5. Method according to claim 1, characterized in that when the phase-locked loop comprises a frequency divider (11) through which the input signal is applied to the phase detector (13), the counter of the frequency divider is reset in response to a change causing a currently used input signal to become inadequate for locking, and

in response to a change causing a currently used input signal to become adequate for locking, the counter of the frequency divider is enabled so that the phase difference between the input signals of the phase detector immediately corresponds to the nominal phase shift of the phase detector.

6. Phase-locked loop comprising a phase detector (13), a loop filter (14) and a voltage-controlled oscillator (15) connected in succession, a feedback path being established from the output of the oscillator to a second input (I2) in the phase detector, and a first input of said phase detector forming an input for an input signal to which the loop is locked,

means (21) for freezing a signal connected from the loop filter (14) to the oscillator (15) to a constant value, and

feedback means (25; 45) fed back from the output

of the loop filter so that an additional feedback path can be established for the phase-locked loop, the additional feedback path being operationally connected to maintain the output signal of the loop filter (14) substantially at said constant value,

characterized in that the connection between the phase detector and the loop filter is maintained when said additional feedback path is operative, and

the phase-locked loop further comprises means (11) for disabling said input signal before said phase detector.

7. Phase-locked loop according to claim 6, characterized in that said means for freezing the signal connected to the oscillator (15) to a constant value comprise a sampling circuit (21) including means for calculating the constant value on the basis of sample values.

8. Phase-locked loop according to claim 7, characterized in that said feedback means for maintaining the loop filter at said constant value comprise a feedback amplifier (22) having a first input connected to the output of the loop filter, a second input connected to the output of said sampling circuit (21), and an output which is operationally connected to provide DC control voltage for the loop filter.

9. Phase-locked loop according to claim 8, characterized in that said feedback means for maintaining the loop filter at said constant value further comprise a sampling circuit (23) arranged between the feedback amplifier (22) and the filter (14), the value of the output signal of the sampling circuit being freezable to a constant value.

10. Phase-locked loop according to claim 7,

c h a r a c t e r i z e d in that said feedback means for maintaining the loop filter at said constant value comprise a comparator (32) having a first input connected to the output of the loop filter (14) and a
5 second input connected to the output of said sampling circuit (21), and an adjustable voltage supply (33), the output signal of the comparator being connected to control the voltage supply, whereby the output of the voltage supply provides DC control voltage for the
10 loop filter (14).

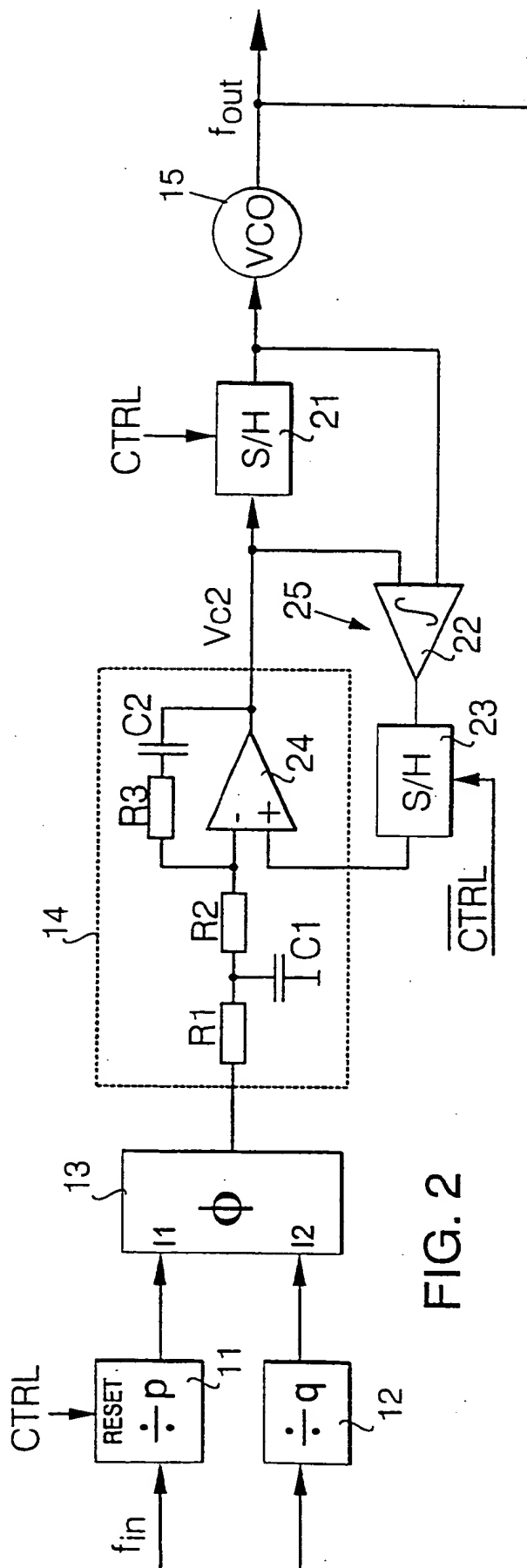
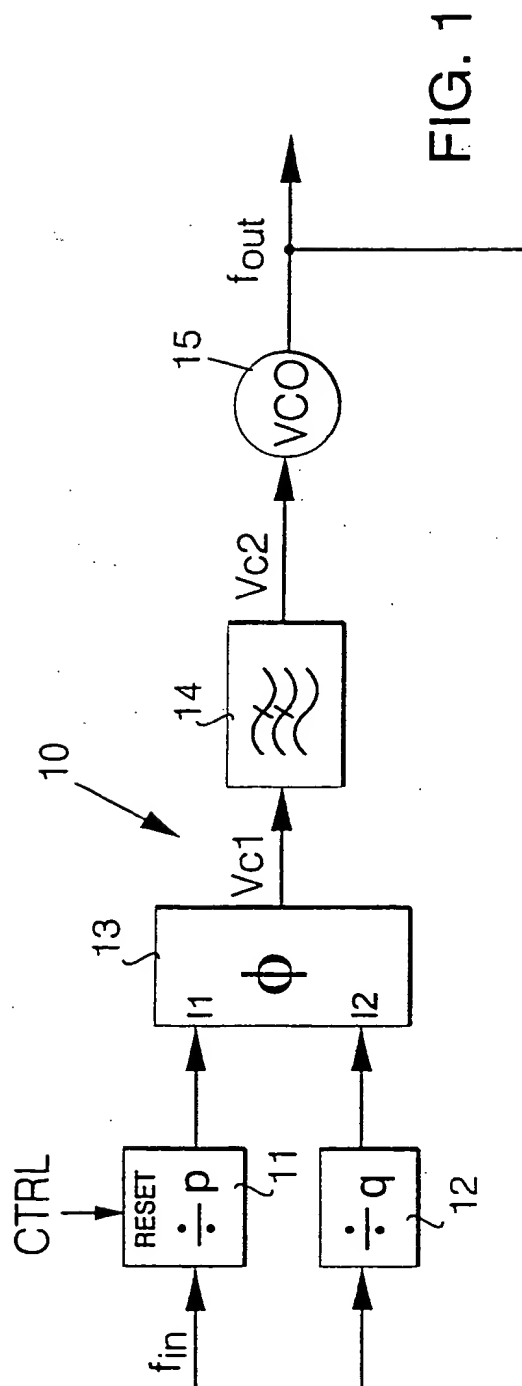
11. Phase-locked loop according to claim 10, c h a r a c t e r i z e d in that the adjustable voltage supply (33) comprises means for generating a signal having an adjustable pulse ratio, and means for
15 lowpass-filtering said signal.

12. Phase-locked loop according to claim 10, c h a r a c t e r i z e d in that the adjustable voltage supply (33) comprises an up/down counter and a D/A converter, which is controlled by the counter.

20 13. Phase-locked loop according to claim 7, c h a r a c t e r i z e d in that said feedback means for maintaining the loop filter at said constant value comprise a comparator (32) having a first input connected to the output of the loop filter (14) and a
25 second input connected to the output of said sampling circuit (21), and the output of which is connected to phase-adjusting means (40) provided at the input of the phase detector (13) for adjusting the mutual phase of signals fed to the phase detector.

30 14. Phase-locked loop according to claim 6, c h a r a c t e r i z e d in that it further comprises means (26, 27) for adding a low offset voltage to the input of the loop filter.

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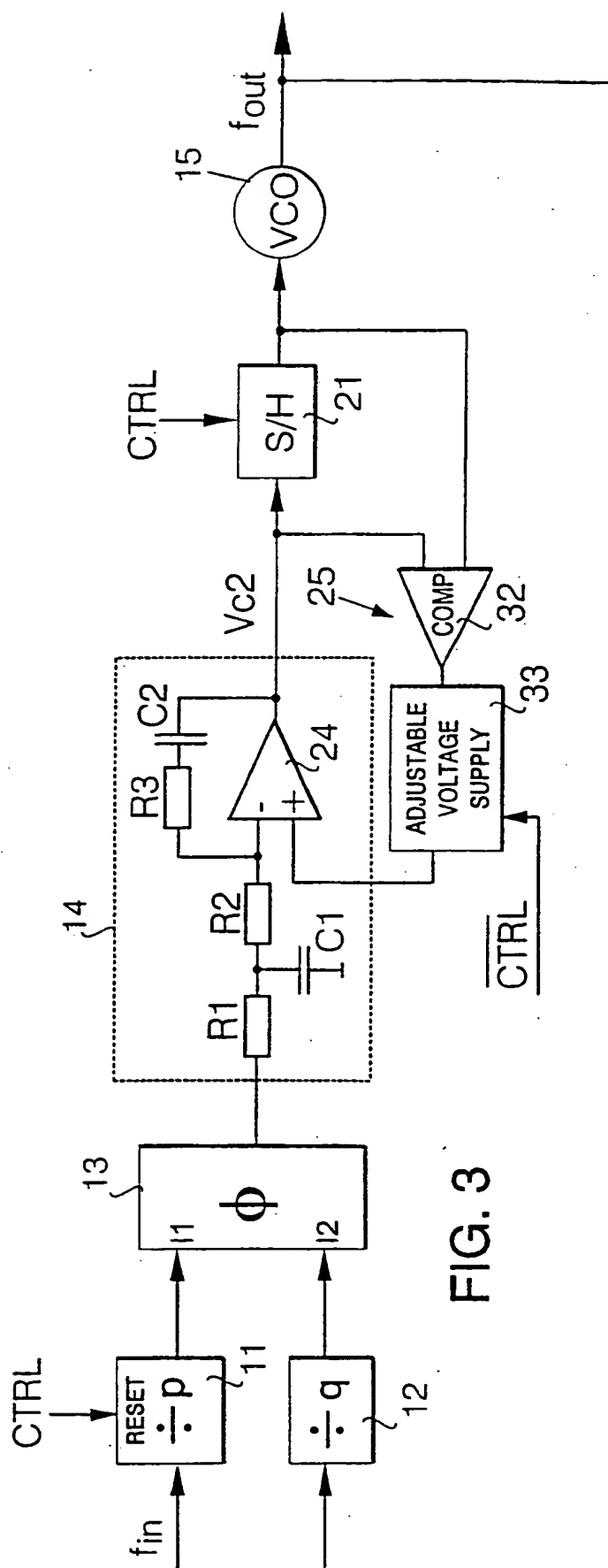


FIG. 3

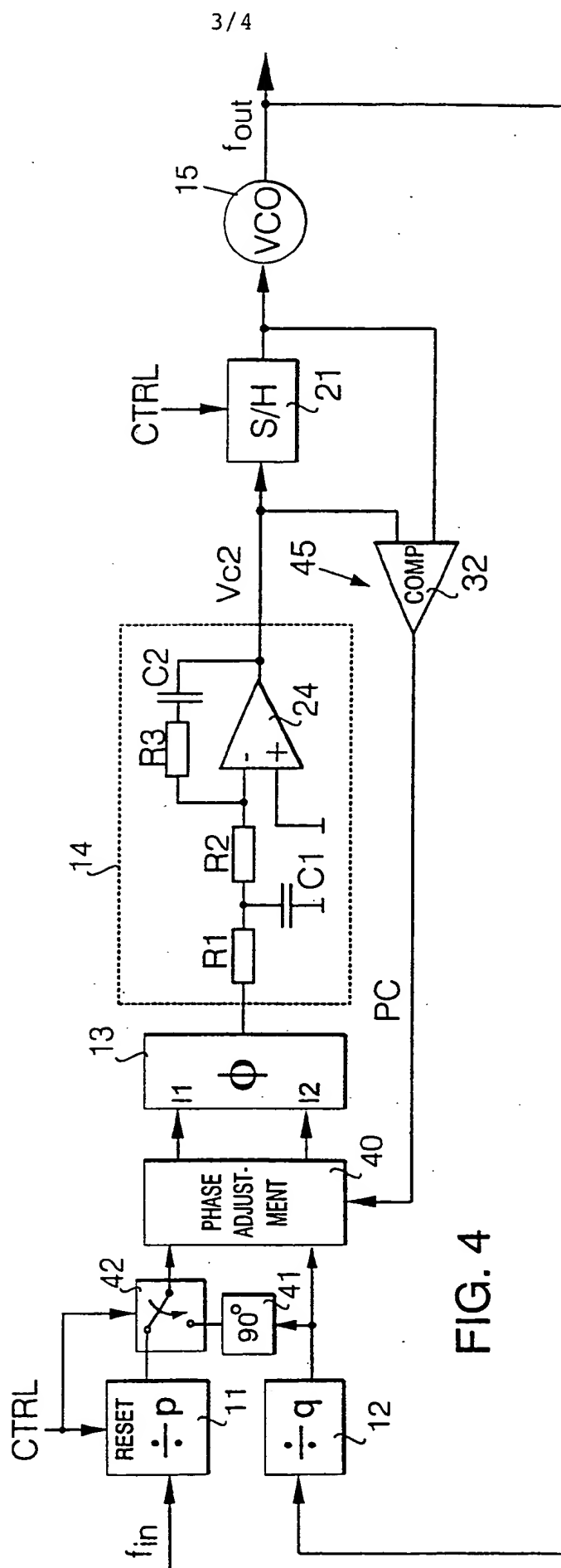


FIG. 4

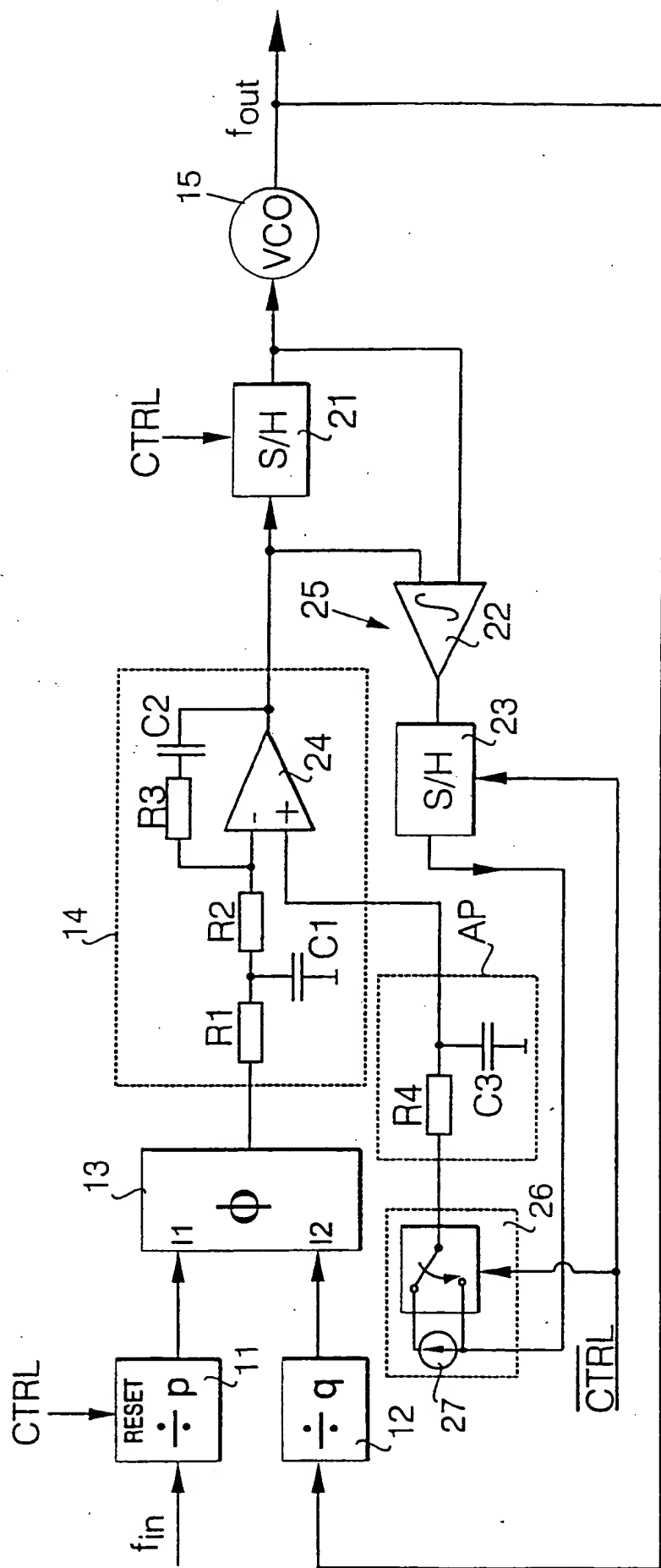


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.

PCT/FI 94/00432

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H03L 7/14, H03L 7/091

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: H03L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CLAIMS, WPI

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	Patent Abstracts of Japan, Vol. 12, No 324, E-653, abstract of JP, A, 63-90216 (MATSUSHITA ELECTRIC IND CO LTD), 21 April 1988 (21.04.88) --	1,2,6,7
A	US, A, 3903482 (FERRUCCIO PAUSINI ET AL), 2 Sept 1975 (02.09.75), figure 1, abstract --	1,6
A	EP, A2, 0320748 (BULL HN INFORMATION SYSTEMS), 21 June 1989 (21.06.89), abstract --	1,6

☒ Further documents are listed in the continuation of Box C.☒ See patent family annex.

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Date of the actual completion of the international search

21 December 1994

Date of mailing of the international search report

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INTERNATIONAL SEARCH REPORT

International application No.

PCT/FI 94/00432

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 4531102 (JONATHAN B. WHITLOCK ET AL), 23 July 1985 (23.07.85), abstract -----	1,6

INTERNATIONAL SEARCH REPORT

Information on patent family members

26/11/94

International application No.

PCT/FI 94/00432

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
US-A-	3903482	02/09/75	DE-A-	2428495	02/01/75
			SE-B,C-	392374	21/03/77
			SE-A-	7407745	19/12/74

EP-A2-	0320748	21/06/89	DE-A-	3878539	25/03/93
			US-A-	4918404	17/04/90

US-A-	4531102	23/07/85	CA-A-	1206218	17/06/86

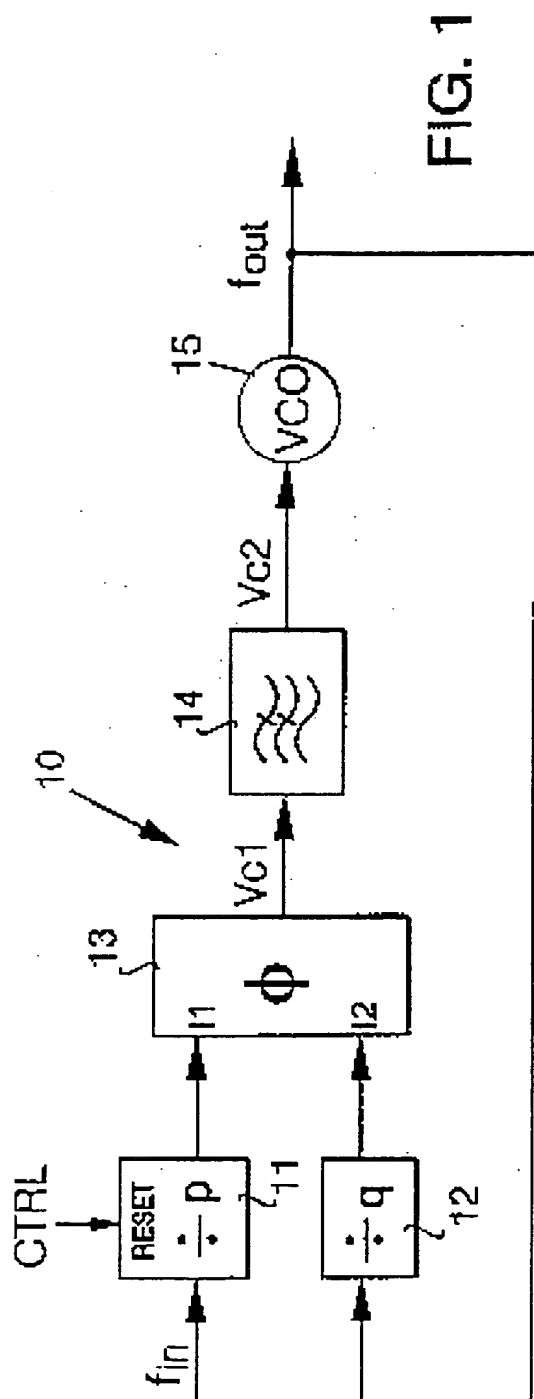


FIG. 1

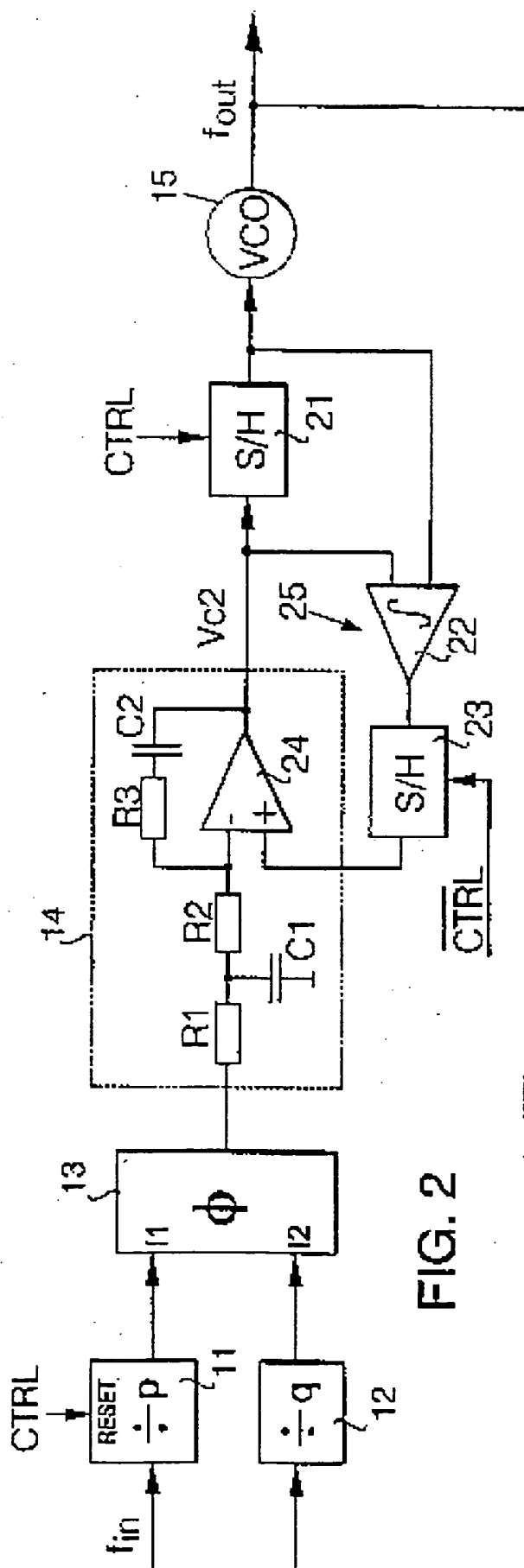


FIG. 2

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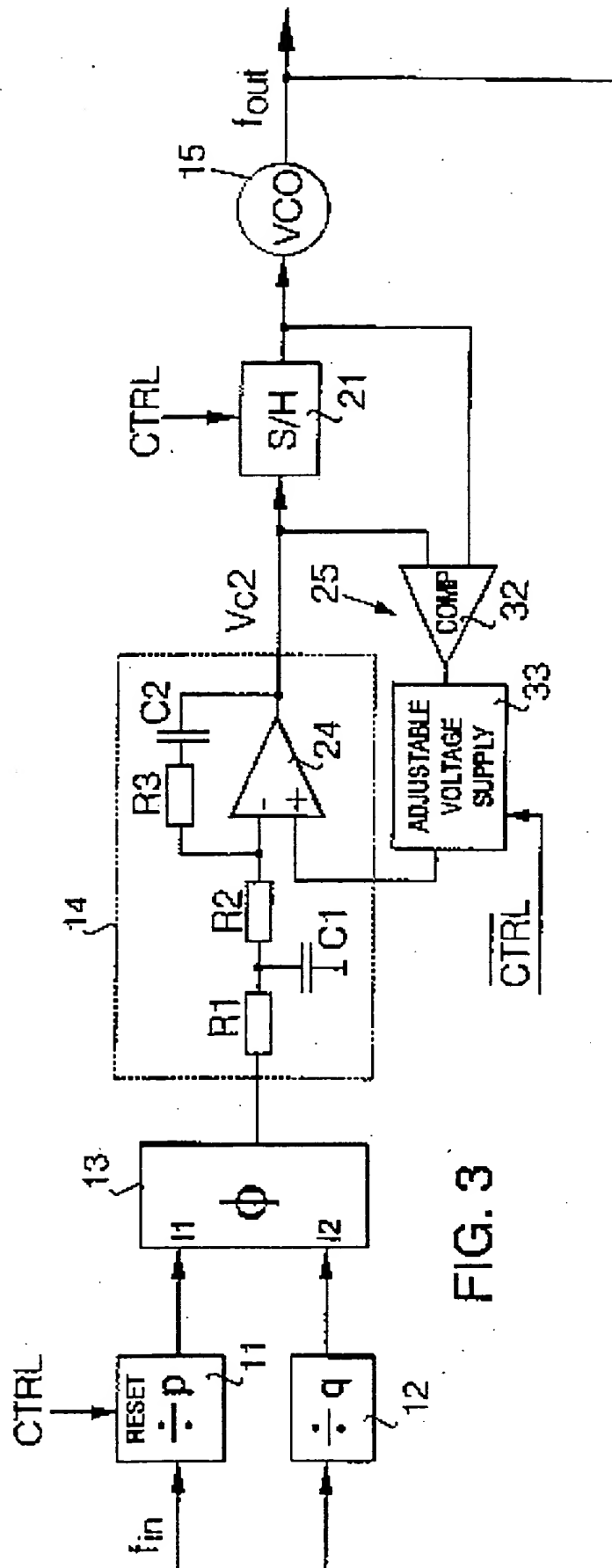


FIG. 3

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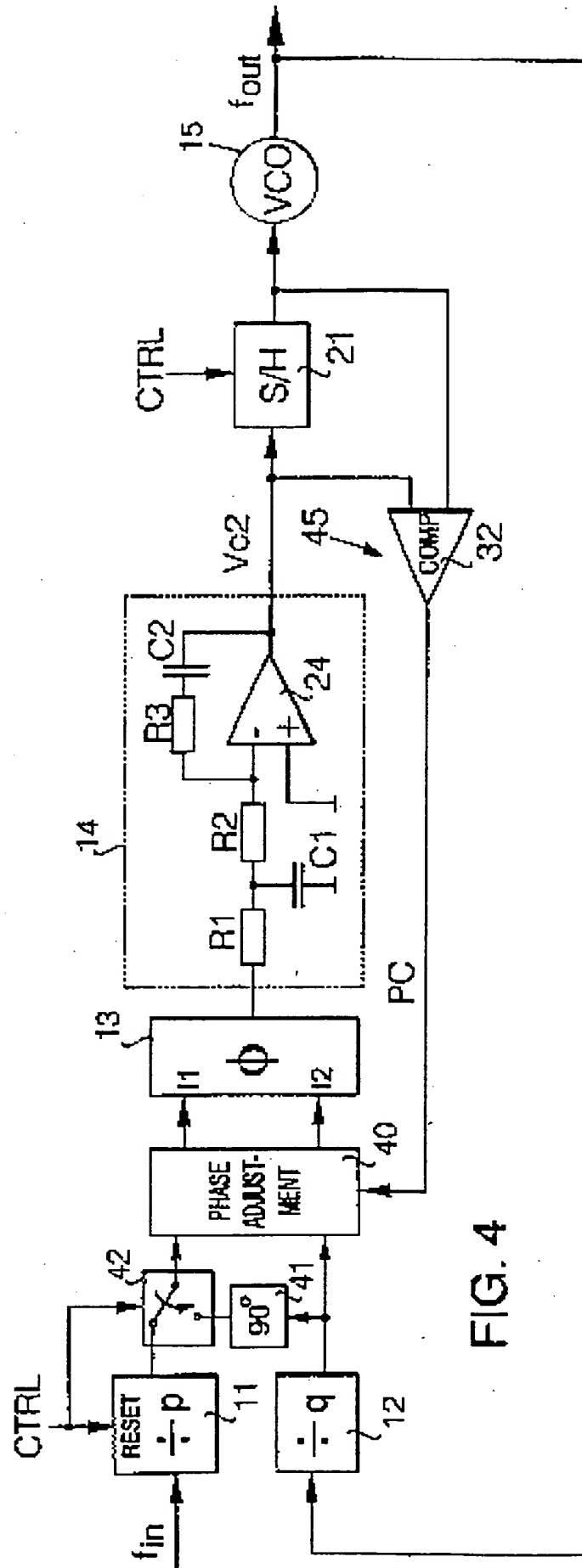


FIG. 4

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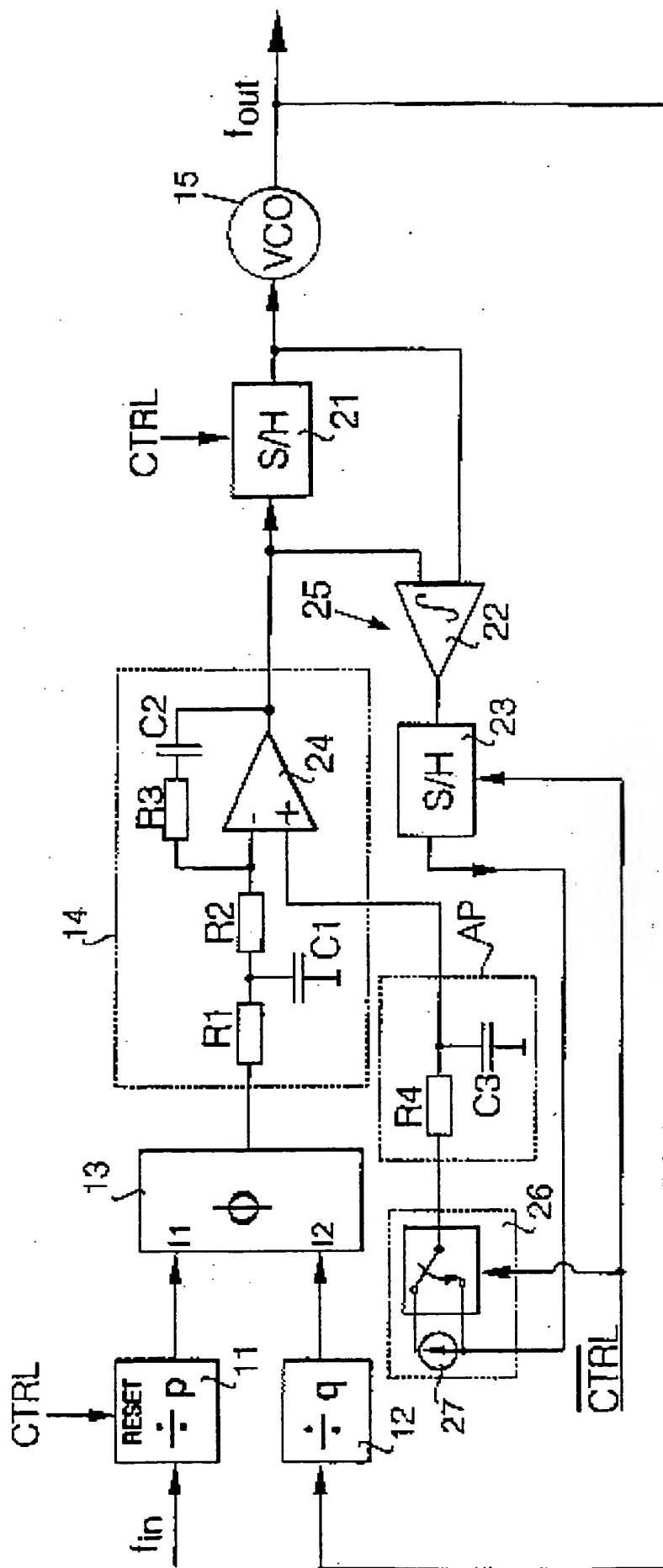


FIG. 5